



CE-ATA Technical Errata

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| Errata ID | Protocol 015 |
| Affected Spec Ver. | Protocol 1.0 |
| Corrected Spec Ver. | |

Submission info

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| Name | Company | Date |
| Amber Huffman | Intel | 08/30/2005 |

Description of the specification technical flaw (add space as needed)

The MMC command layer state machine did not make clear that the R4 register data contents are only valid on FAST_IO (CMD39) read requests. This erratum clarifies that the Register Read Contents field is filled in when WR=0 (specifying a read) and leaves the contents of this field unspecified for writes.

Description of the correction

State DC15: DC_Cmd39_R4 in section 2.4.2.1.2 shall be modified as shown:

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|-------------------|--|---------------|
| DC15: DC_Cmd39_R4 | Transmit R4 response with Register Read Contents Data filled in based on current contents of Register Address if WR=0 (R) . If WR=1 (W), notify ATA layer of register write. | |
| 1. | R4 response transmission complete | → DC_Idle |
| 2. | R4 response transmission not complete | → DC_Cmd39_R4 |

Disposition log

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| 08/30/2005 | Erratum captured |
| 09/13/2005 | Replaced erroneous "State DC7:..." with "State DC15..." text prior to state. |
| 11/14/2005 | Erratum ratified |

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